WHAT IS CLAIMED IS:

1. An amplifier circuit, comprising:

a first stage and a second stage, the first stage comprising a quad configuration and the second stage comprising a translinear current amplifier configuration; and

a coupling circuit operably coupling the first stage and the second stage to reduce transistor beta loading effects.

2. The amplifier circuit recited in Claim 1, wherein the first stage quad configuration is modified using emitter degeneration.

3. The amplifier circuit recited in Claim 1, wherein the current gain of the second stage is given by:

$$(I A_{out\,1} - I A_{out\,2})/(I_{out1} - I_{out2}) = (1 + R_{123} / R_{124}) \cdot (I_{135} / I_{134}) \cdot (A / (1+A))$$

where $A = g_{m\,Q109} \cdot R_{124}$;

IA_{out1} is the amplified output collector current from Q_{110};

IA_{out2} is the output collector current from transistor Q_{111};

I_{out1} is the output current from Q_{103} and Q_{105} from the first stage quad, and I_{out2} is the collector current from Q_{104} and Q_{106} from the first stage quad;

R_{123} is the resistance value of the third resistor and R_{124} is the resistance value of the fourth resistor;

I_{135} is the current through the fifth current source; and

I_{134} is the value of the current through the fourth current source.

4. The amplifier circuit recited in Claim 1, further comprising current to voltage conversion and common mode feedback in the second stage operable to provide high speed, low distortion and extended bandwidth.

5. The amplifier circuit recited in Claim 1, wherein the amplifier is formed of complementary bipolar devices.

6. The amplifier circuit recited in Claim 1 being adapted for use in an integrated circuit.

7. The amplifier circuit recited in Claim 1 being adapted for use in a variable gain amplifier.

8. An amplifier circuit, comprising a first stage and a second stage, the first stage comprising a quad configuration, and the second stage comprising a resistive shunt current feedback amplifier with a Darlington/level shift input stage operable to reduce transistor beta loading effects.

9. The amplifier circuit recited in Claim 8, wherein the first stage quad is modified using emitter degeneration.

10. An amplifier circuit, comprising:

a first stage quad operable to bias transistors; and

a coupling circuit coupling the first stage quad to a second stage translinear current amplifier operable to reduce transistor beta loading effects and provide improved slew rate, low distortion and extended bandwidth.

11. The amplifier circuit recited in Claim 10, wherein the first stage quad is modified using emitter degeneration.

12. An amplifier circuit, comprising:

a first stage comprising six transistors, two resistors and a current source configured as a quad;

a second stage comprising eight transistors, four resistors, and six current sources configured as a translinear current amplifier;

the first stage being coupled to the second stage operable to provide current gain of:

$$(IA_{out1} - IA_{out2}) / (I_{out1} - I_{out2}) = (1 + R_{123} / R_{124}) \cdot (I_{135} / I_{134}) \cdot (A / (1+A))$$

where $A = g_{mQ109} \cdot R_{124}$;

IA_{out1} is the amplified output collector current from Q_{110};

IA_{out2} is the output collector current from transistor Q_{111};

I_{out1} is the output current from Q_{103} and Q_{105} from the first quad stage quad, and I_{out2} is the collector current from Q_{104} and Q_{106} from the first quad stage;

R_{123} is the resistance value of the third resistor and R_{124} is the

resistance value of the fourth resistor;

I_{135} is the current through the fifth current source; and

I_{134} is the value of the current through the fourth current source.

13. The amplifier circuit recited in Claim 12 wherein the first stage quad is modified using emitter degeneration.

14. The amplifier circuit recited in Claim 12, further comprising:

the first stage comprising two input voltage nodes, a first input voltage node being coupled to the base of a first transistor, a second input voltage node being coupled to the base of a second transistor;

the emitter of the first transistor being coupled to the first terminal of a first resistor, the second terminal of the first resistor being coupled to the first node of a first current source and the second node of the first current source being coupled to a ground reference;

the emitter of the second transistor being coupled to the first terminal of a second resistor, the second terminal of the second resistor being coupled to the first node of the first current source;

the collector of the first transistor being coupled to the emitter of a third transistor, the emitter of a fourth transistor being coupled to the collector of the first transistor, the collector of the third transistor being coupled to a first current output node of the first stage;

the collector of the fourth transistor being coupled to a second output current node of the first stage;

the base of the third transistor being coupled to the base of a sixth transistor;

the base of the fourth transistor being coupled to the base of a fifth transistor;

the node coupling the base of the third transistor and the base of the sixth transistor having a first input control node;

the node coupling the base of the fourth transistor and the base of the fifth transistor being coupled to a second control input node;

the collector of the second transistor being coupled to the emitter of the fifth transistor and the emitter of the sixth transistor, the collector of the fifth transistor being coupled to the first output current node of the first stage, the collector of the sixth transistor being coupled to a second output current node of the first stage;

the second stage comprising the base of a seventh transistor being coupled to the second output current node of the first stage, the emitter of the seventh transistor being coupled to a first node of the second current source and the base of an eighth transistor, the second node of the second current source being coupled to the ground reference;

the collector of the seventh transistor being coupled to a voltage supply rail and the collector of the eighth transistor being coupled to the voltage supply rail;

the second output current node from the first stage being coupled to a first terminal of a third resistor, the second terminal of the third resistor being coupled to the collector of a ninth transistor, the base of the ninth transistor being coupled to the

emitter of the eighth transistor, the base of the ninth transistor also being coupled to a first terminal of a third current source;

the second terminal of the third current source being coupled to the ground reference, the first terminal of the third current source also being coupled to the base of a tenth transistor;

the emitter of the ninth transistor being coupled to a first terminal of a fourth current source, a second terminal of the fourth current source being coupled to the ground reference;

the collector of the ninth transistor also being coupled to a first terminal of a fourth resistor, a second terminal of the fourth resistor being coupled to the voltage supply rail;

the emitter of the tenth transistor being coupled to a first terminal of a fifth current source, a second terminal of the fifth current source being connected to the ground reference, the emitter of the ninth transistor also being coupled to the emitter of a twelfth transistor;

the emitter of the tenth transistor also being coupled to the emitter of an eleventh transistor, the base of the eleventh transistor being coupled to a first terminal of a sixth current source, a second terminal of the sixth current source being coupled to the ground reference;

the base of the twelfth transistor also being coupled to the first terminal of the sixth current source;

the emitter of a thirteenth transistor being coupled to the first terminal of the sixth current source;

the collector of the twelfth transistor being coupled to a first terminal of a fifth resistor, a second terminal of the fifth resistor being coupled to the voltage supply rail;

the collector of the thirteenth transistor being coupled to the voltage supply rail, the base of a fourteenth transistor being coupled to the first output current node of the first stage, the base of the fourteenth transistor also being coupled to a first terminal of a sixth resistor, a second terminal of the sixth resistor being coupled to the collector of the twelfth transistor;

the collector of the fourteenth transistor being coupled to the voltage supply rail, the emitter of the fourteenth transistor being coupled to a first terminal of a seventh current source, the second terminal of the seventh current source being coupled to the ground reference;

the emitter of the fourteenth transistor also being coupled to the base of the thirteenth transistor;

the collector of the tenth transistor being coupled to a node operable as an output current node of the second stage; and

the collector of the eleventh transistor being coupled to a node operable as an output current node of the second stage.

15. The amplifier circuit recited in Claim 14, wherein the first, second, third, fourth, fifth, sixth, seventh, eighth, ninth, tenth, eleventh, twelfth, thirteenth and fourteenth transistors comprise npn transistors.

16. The amplifier circuit recited in Claim 14 being adapted for use in an integrated circuit.

17. The amplifier circuit recited in Claim 14 being adapted for use as a variable gain amplifier.